Listing of claims:

1. (Currently Amended) An apparatus, comprising:

a first stage circuit that includes an array of amplifier circuits, wherein each of the amplifier circuits includes: an offset adjustment circuit, an output that is coupled to a common node, an input that is arranged to receive a feedback signal, and a null control input that is arranged to receive a respective null control signal such that ~~the~~ each respective offset adjustment circuit is arranged to remove a respective input referred offset for a respective one of the amplifier circuits ~~is responsive to the~~ in response to each respective null control signal, wherein each respective null control signal is independent of one another;

a second stage circuit that is arranged to provide a reference signal to an output node in response to an intermediate signal that is associated with the common node;

a feedback circuit that is arranged to provide the feedback signal in response to the reference signal, wherein the feedback circuit includes a band-gap core circuit, wherein the band-gap core circuit comprises: a first bipolar junction transistor that is arranged in a common-base configuration with a second bipolar junction transistor, and a resistor that is coupled to the second bipolar junction transistor, wherein the first bipolar junction transistor has a first base-emitter voltage given as VBE1, the second bipolar junction transistor has a second base-emitter voltage given as VBE2, and a voltage across the resistor is given as delta VBE, wherein the first stage circuit, the second stage circuit, and the feedback circuit are arranged for closed-loop operation with the band-gap core circuit such that VBE1 = VBE2 + delta VBE; and

a null control logic circuit that is arranged to provide a set of null control signals, where each null control signal is associated with a respective one of the amplifier circuits such that the amplifier circuits are selectively zeroed to minimize the effects of offset in each of the amplifier circuits.

2. (Original) The apparatus of Claim 1, wherein each of the amplifier circuits in the first stage circuit includes a differential pair circuit, wherein each differential pair circuit comprises at

least one of: an n-type transistor pair, a p-type transistor pair, a FET type transistor pair, and a BJT type transistor pair.

3. (Original) The apparatus of Claim 1, wherein at least one of the amplifier circuits includes a trans-conductance cell, wherein the trans-conductance cell comprises: a differential pair circuit that is coupled to a current mirror circuit, wherein the differential pair circuit is arranged to: receive a differential signal from a first node and a second node, and provide at least a portion of the intermediate signal to the common node in response to the differential signal.

4. (Original) The apparatus of Claim 1, wherein at least one of the amplifier circuits includes a switching circuit that is arranged to selectively zero the offset voltage associated with the trans-conductance cell in response to a selected one of the null control signals.

5. (Currently Amended) ~~The apparatus of Claim 1,~~ An apparatus, comprising:

a first stage circuit that includes an array of amplifier circuits, wherein each of the amplifier circuits includes: an offset adjustment circuit, an output that is coupled to a common node, an input that is arranged to receive a feedback signal, and a null control input that is arranged to receive a respective null control signal such that the offset adjustment circuit for a respective one of the amplifier circuits is responsive to the respective null control signal;

a second stage circuit that is arranged to provide a reference signal to an output node in response to an intermediate signal that is associated with the common node;

a feedback circuit that is arranged to provide the feedback signal in response to the reference signal, wherein the feedback circuit includes a band-gap core circuit; and

a null control logic circuit that is arranged to provide a set of null control signals, where each null control signal is associated with a respective one of the amplifier circuits such that the amplifier circuits are selectively zeroed to minimize the effects of offset in each of the amplifier circuits, wherein at least one of the amplifier circuits comprises:

a trans-conductance cell, wherein the trans-conductance cell comprises: a differential pair circuit that is coupled to a current mirror circuit, wherein the differential pair

circuit is arranged to: receive a differential signal from a first node and a second node, and provide at least a portion of the intermediate signal to the common node in response to the differential signal; and

a switching circuit that is arranged to selectively zero the offset voltage associated with the trans-conductance cell in response to a selected null control signals.

6. (Original) The apparatus of Claim 5, wherein the switching circuit is further arranged to selectively couple the differential signal across the first node and the second node when the selected null control signal is deasserted.

7. (Original) The apparatus of Claim 5, wherein the switching circuit is further arranged to selectively couple the first and second nodes together when the selected null control signal is asserted.

8. (Original) The apparatus of Claim 5, wherein the switching circuit is further arranged to selectively couple the differential signal across the first node and the second node when the selected null control signal is deasserted, and also arranged to selectively couple the first and second nodes together when another selected null control signal is asserted.

9. (Original) The apparatus of Claim 8, wherein the switching circuit is further arranged to: selectively couple a first capacitor to the third node when the other null control signal is asserted, and selectively couple a second capacitor to the common node when the other null control signal is asserted.

10. (Previously Presented) An apparatus comprising:

a first stage circuit that includes an array of amplifier circuits, wherein each of the amplifier circuits includes: an offset adjustment circuit, an output that is coupled to a common node, an input that is arranged to receive a feedback signal, and a null control input that is arranged to receive a respective null control signal such that the offset adjustment circuit for a

respective one of the amplifier circuits is responsive to the respective null control signal; wherein at least one of the amplifier circuits includes a trans-conductance cell that comprises:

a first transistor that includes a source that is coupled to a seventh node, a gate that is coupled to a first node, and a drain that is coupled to a third node;

a second transistor that includes a source that is coupled to the seventh node, a gate that is coupled to the second node, and a drain that is coupled to the common node;

a third transistor that includes a source that is coupled to a power supply node, a gate that is coupled to the third node, and a drain that is coupled to the common node;

a fourth transistor that includes a source that is coupled to the power supply node, and a gate and drain that are coupled to the third node; and

a fifth transistor that is arranged to operate as a current source that is coupled to the seventh node

a second stage circuit that is arranged to provide a reference signal to an output node in response to an intermediate signal that is associated with the common node;

a feedback circuit that is arranged to provide the feedback signal in response to the reference signal, wherein the feedback circuit includes a band-gap core circuit; and

a null control logic circuit that is arranged to provide a set of null control signals, where each null control signal is associated with a respective one of the amplifier circuits such that the amplifier circuits are selectively zeroed to minimize the effects of offset in each of the amplifier circuits.

11. (Original) The apparatus of Claim 10, further comprising:

a sixth transistor that include a source that is coupled to the power supply node, a gate that is coupled to a sixth node, and a drain that is coupled to the common node;

a seventh transistor that include a source that is coupled to the power supply node, a gate that is coupled to a fifth node, and a drain that is coupled to the third node;

a first capacitor that is coupled between the fifth node and the power supply node;

a second capacitor that is coupled between the sixth node and the power supply node;

a fourth switching transistor that is arranged to selectively couple the fifth node to the third node when actuated; and

a fifth switching transistor that is arranged to selectively couple the sixth node to the common node when actuated.

12. (Original) The apparatus of Claim 11, further comprising.

a first switching transistor that is arranged to couple the feedback signal to the first node when actuated;

a second switching transistor that is arranged to couple a reference signal to the second node when actuated; and

a third switching transistor that is arranged to couple the first node to the second node when actuated.

13. (Original) The apparatus of Claim 1, wherein the first stage circuit, the second stage circuit, the feedback circuit, and the feedback circuit are configured to operate as at least one of: a switching regulator circuit, a reference voltage circuit, a low drop out (LDO) regulator circuit, and a band-gap reference circuit.

14. (Previously Presented) An apparatus comprising:

a first stage circuit that includes an array of amplifier circuits, wherein each of the amplifier circuits includes: an offset adjustment circuit, an output that is coupled to a common node, an input that is arranged to receive a feedback signal, and a null control input that is arranged to receive a respective null control signal such that the offset adjustment circuit for a respective one of the amplifier circuits is responsive to the respective null control signal;

a second stage circuit that is arranged to provide a reference signal to an output node in response to an intermediate signal that is associated with the common node;

a feedback circuit that is arranged to provide the feedback signal in response to the reference signal, wherein the feedback circuit includes a band-gap core circuit, wherein the band-gap core circuit comprises: a first transistor that is coupled between a power supply node and an eight node, a second transistor that is coupled between the power supply node and a ninth node, a first resistor that is coupled between the eighth node and a tenth node, a second resistor that is coupled between the tenth node and the output node, and a third resistor that is coupled between the ninth node and the output node, wherein the feedback signal is associated with at least one of the ninth node and the tenth node; and

a null control logic circuit that is arranged to provide a set of null control signals, where each null control signal is associated with a respective one of the amplifier circuits such that the amplifier circuits are selectively zeroed to minimize the effects of offset in each of the amplifier circuits.

15. (Currently Amended) An apparatus, comprising:

a first amplifier means that includes a first offset adjustment circuit, a first output that is coupled to a common node, a first input that is arranged to receive a feedback signal, and a first null control input that is arranged to couple a first null control signal to the first offset adjustment circuit such that the first offset adjustment circuit is arranged to remove a first input referred offset associated with the first amplifier means in response to the first null control signal;

a second amplifier means that includes a second offset adjustment circuit, a second output that is coupled to the common node, a second input that is arranged to receive the feedback signal, and a second null control input that is arranged to couple a second null control signal to the second offset adjustment circuit such that the second offset adjustment circuit is arranged to remove a second input referred offset associated with the second amplifier means in response to the second null control signal;

a third amplifier means that includes a third offset adjustment circuit, a third output that is coupled to the common node, a third input that is arranged to receive the feedback signal, and a third null control input that is arranged to couple a third null control signal to the

third offset adjustment circuit such that the third offset adjustment circuit is arranged to remove a third input referred offset associated with the third amplifier means in response to the third null control signal, wherein the first, second, and third null control signals are independent of one another;

a second stage means that is arranged to provide a reference signal in response to an intermediate signal, wherein the intermediate signal is associated with the common node;

a feedback means that is arranged to provide the feedback signal in response to the reference signal, wherein the feedback means includes a band-gap core means, wherein the band-gap core means comprises: a first bipolar junction transistor that is arranged in a common-base configuration with a second bipolar junction transistor, and a resistor that is coupled to the second bipolar junction transistor, wherein the first bipolar junction transistor has a first base-emitter voltage given as VBE1, the second bipolar junction transistor has a second base-emitter voltage given as VBE2, and a voltage across the resistor is given as delta VBE, wherein the first stage circuit, the second stage circuit, and the feedback circuit are arranged for closed-loop operation with the band-gap core means such that VBE1 = VBE2 + delta VBE; and

a null control means that is arranged to provide the first, second, and third null control signals such that an offset voltage associated with one of the first, second, and third amplifiers means is selectively zeroed in response to the respective one of the first,-second, and third null control signals while the others of the first, second, and third amplifier means are not zeroed.

16. (Original) The apparatus of Claim 15, wherein the null control means comprises at least one of a shift register, a barrel shifter, a counter, an oscillator, a randomizer, and a power-on-reset circuit.

17. (Original) The apparatus of Claim 15, wherein the null control means is further arranged to activate one of the first and second null control signals at a time.

18. (Previously Presented) The apparatus of Claim 15, wherein the third amplifier means includes a third output that is coupled to the common node, a third input that is arranged to receive the feedback signal, and a third null control input that is arranged to receive a third null control signal, wherein the null control means is further arranged to provide the third control signal such that the offset voltage associated with each of the first, second, and third amplifier means are selectively zeroed in response to the respective one of the first, second, and third null control signals.

19. (Original) The apparatus of Claim 18, wherein the null control means is further arranged to assert one of the first, second, and third null control signals when the others of the first, second, and third null control signals are deasserted.

20. (Currently Amended) A method for reducing the offset voltage associated with a reference signal, comprising:

coupling together the outputs from an array of amplifier circuits at a common node to provide an intermediate signal, wherein each of the amplifier circuits includes an offset adjustment circuit therein;

coupling the common node to a second stage circuit;

generating the reference signal as an output of the second stage circuit that is responsive to the intermediate signal;

providing a feedback signal to the array of amplifier circuits in response to the reference signal, wherein the feedback signal is associated with a band-gap core circuit, wherein the band-gap core circuit comprises: a first bipolar junction transistor that is arranged in a common-base configuration with a second bipolar junction transistor, and a resistor that is coupled to the second bipolar junction transistor, wherein the first bipolar junction transistor has a first base-emitter voltage given as VBE1, the second bipolar junction transistor has a second base-emitter voltage given as VBE2, and a voltage across the resistor is given as delta VBE;

selecting one of the array of amplifier circuits for offline operation;

nulling an offset voltage associated with the selected amplifier circuit while the selected amplifier circuit is in offline operation;

controlling the non-selected amplifier circuits with the feedback signal for closed-loop operation with the band-gap core circuit such that VBE1 = VBE2 + delta VBE; and

maintaining the non-selected amplifier circuits such that the offset voltage associated with the reference signal is zeroed as an average.

21. (Currently Amended) An apparatus that is arranged to provide a reference signal, comprising:

a feedback circuit that is arranged to provide a feedback signal that is responsive to the reference signal, wherein the feedback circuit includes a band-gap core circuit, wherein the band-gap core circuit comprises: a first bipolar junction transistor that is arranged in a common-base configuration with a second bipolar junction transistor, and a resistor that is coupled to the second bipolar junction transistor, wherein the first bipolar junction transistor has a first base-emitter voltage given as VBE1, the second bipolar junction transistor has a second base-emitter voltage given as VBE2, and a voltage across the resistor is given as delta VBE;

an output circuit that is arranged to provide the reference signal in response to an output control signal;

a null control logic circuit that is arranged to provide a first control signal, a second control signal, and a third control signal such that one of the first, second, and third control signals is asserted while the other of the first, second, and third control signals is deasserted; and

an error amplifier circuit that is arranged to provide the output control signal in response to the feedback signal and another reference signal, wherein the feedback circuit, the output circuit, and the error amplifier circuit are arranged for closed-loop operation with the band-gap core means such that VBE1 = VBE2 + delta VBE, wherein the error amplifier circuit comprises:

a first amplifier circuit that includes a first inverting input that is coupled to a first node, a first non-inverting input that is coupled to a second node, a first output

that is coupled to a common node, and a first control input that is arranged to receive the first control signal;

a first offset adjustment circuit that is integrally formed with the first amplifier circuit, wherein the first offset adjustment circuit is enabled in response to the first control signal;

a second amplifier circuit that includes a second inverting input that is coupled to the first node, a second non-inverting input that is coupled to the second node, a second output that is coupled to the common node, and a second control input that is arranged to receive the second control signal;

a second offset adjustment circuit that is contained within the second amplifier circuit, wherein the second offset adjustment circuit is enabled in response to the second control signal;

a third amplifier circuit that includes a third inverting input that is coupled to the first node, a third non-inverting input that is coupled to the third node, a third output that is coupled to the common node, and a third control input that is arranged to receive the third control signal;

a third offset adjustment circuit that is contained within the third amplifier circuit, wherein the third offset adjustment circuit is enabled in response to the third control signal, wherein: the feedback signal is coupled to one of the first and second nodes, ~~and~~ the other reference signal is coupled to an other of the first and second node, and the first, second, and third control signals are operated independent of one another; and

a second stage amplifier circuit that is arranged to provide the output control signal in response to an intermediate signal that is associated with the common node.